An Ultra Broadband GaAs MESFET Preamplifier IC for a 10 Gb/s Optical Communication System

Miyo Miyashita, Kosei Maemura, Kazuya Yamamoto, Teruyuki Shimura, Masamichi Nogami, Kuniaki Motoshima, Tadayoshi Kitayama, and Yasuo Mitsui

Abstract—**An ultra broadband GaAs MESFET preamplifier IC has been developed for a 10 Gb/s optical communication system. High transimpedance of 44 dBΩ has been obtained over dc to 12 GHz. A receiver has also been fabricated by using this preamplifier IC and a photodiode. The receiver operates with extremely low equivalent input noise current of 12.6 pA/√Hz over dc to 7.8 GHz. This paper describes circuit design and high frequency characteristics of both the preamplifier IC and the receiver.**

Introduction

A HIGH SPEED and broadband optical communication system useful not only for telecommunication but also for large capacity data and image transmission has increasingly been demanded in realizing the next generation of Broadband Integrated Services Digital Network (B-ISDN). Up to now, a 2.4 Gb/s system has almost come up to practical use and a system with transmission rate of up to 10 Gb/s or more has extensively been studied [1]–[3].

In the fiber optic link, a conventional optical receiver consists of three functional blocks which are equalization, retiming, and regeneration. A preamplifier is a key component in the equalization block and requires low noise and broadband characteristics. Since a preamplifier IC is used with a photodiode in a receiver, the IC has to be designed with consideration of the photodiode's parameters, especially its parasitic capacitance [4].

This paper describes both the circuit design and high frequency characteristics, and superior production controllability in the fabrication process for the preamplifier IC.

Circuit Design

Fig. 1 shows the circuit diagram of the IC. Noise sources in a receiver composed of the IC and a p-i-n-photodiode include thermal noises of the FET and feedback resistor, shot noise due to both the dark current of the p-i-n photodiode and gate leakage current of the FET, and $1/f$ noise.

The dominant noise sources in a receiver are the thermal noises in the input FET and the feedback resistor. These thermal noises depend on total input capacitance of a receiver or feedback resistance. Taking into account the trade-off between noise performance and broad bandwidth, the IC has to be designed so as to get high feedback resistance and low total input capacitance simultaneously.

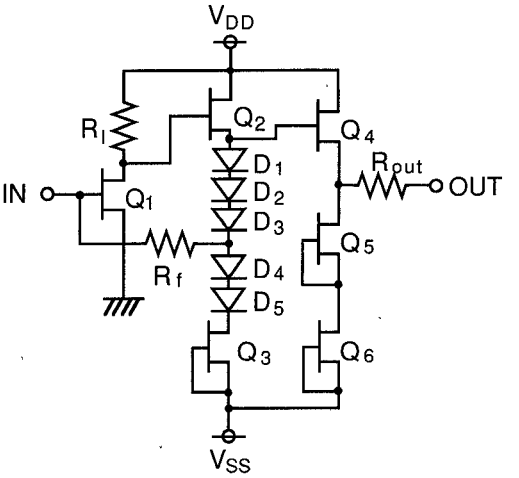


Fig. 1. Circuit diagram of the IC.

The equivalent input noise ($\overline{in^2_{FET}}$) due to thermal noise in the input FET(Q_1) is described by the following equation [5],

$$\overline{in^2_{FET}} = 4kT\Gamma \frac{(\omega \cdot C_t)^2}{g_m} \Delta f. \quad (1)$$

where k is Boltzmann's constant, T is absolute temperature, ω is angular frequency, and g_m is transconductance of the input FET(Q_1). C_t is equal to the sum of the input gate capacitance (C_g) of the input FET and parasitic capacitance (C_{PD}) of the photodiode. Γ is a noise term [5] denoted as follows:

$$\Gamma = P - 2Q\left(\frac{C_g}{C_t}\right) + R\left(\frac{C_g}{C_t}\right)^2 \quad (2)$$

where P, Q, and R are factors depending on various FET parameters and gate bias [5]–[7]. Input noise in the input FET is expressed in (3) where g_{mu} and C_{gu} are transconductance and input gate capacitance per unit gate width.

$$\overline{in^2_{FET}}(W) = 4kT\Gamma(W) \frac{(\omega(C_{PD} + C_{gu} \cdot W))^2}{g_{mu} \cdot W} \Delta f \quad (3)$$

Manuscript received March 31, 1992; revised August 4, 1992.

The authors are with the Optoelectric and Microwave Devices Laboratory, Mitsubishi Electric Corporation, 4-1 Mizuhara, Itami, Hyogo 664, Japan.

IEEE Log Number 9203717.

and

$$\Gamma(W) = P - 2Q\left(\frac{C_{gu}\cdot W}{C_{PD}+C_{gu}\cdot W}\right) + R\left(\frac{C_{gu}\cdot W}{C_{PD}+C_{gu}\cdot W}\right)^2 \quad (4)$$

where W is gate width of the FET(Q_1). In (3), noise current ($\overline{in^2_{FET}}$) is minimized at a condition of

$$W = \sqrt{\frac{P}{P-2Q+R}}\cdot\frac{C_{PD}}{C_{gu}} \simeq 0.7\cdot\frac{C_{PD}}{C_{gu}} \quad (5)$$

where each parameter P, Q, and R for the FET with gate length of 0.5 μm is estimated from a previous report [5] to be 1.105, -0.436, and 0.303, respectively.

On the other hand, the thermal noise of the feedback resistor ($\overline{in^2_{Rf}}$) is expressed by the following equation [8], [9],

$$\overline{in^2_{Rf}} = \frac{4kT}{R_f}\Delta f = \frac{4kT\cdot 2\pi f_{3dB}(C_{PD}+C_{gu}\cdot W)}{A}\Delta f \quad (6)$$

where R_f is the feedback resistance, and A is open loop gain. f_{3dB} is the bandwidth of a receiver consisting of a preamplifier and a photodiode, which is expressed by

$$f_{3dB} = \frac{A}{2\pi R_f(C_{PD}+C_{gu}\cdot W)}. \quad (7)$$

In Fig. 2(a) and (b), two kinds of equivalent input noises ($\overline{in^2_{FET}}$ and $\overline{in^2_{Rf}}$) and total input noise current ($\sqrt{\overline{in^2_t}}$) are plotted against gate width (W), which are obtained by integrating (3) and (6) with respect to frequency from 0 to f_{3dB}. Equivalent total input noise ($\sqrt{\overline{in^2_t}}$) is shown as follows:

$$\sqrt{\overline{in^2_t}} = \left(\left(\int_0^{f_{3dB}}(\overline{in^2_{Rf}}+\overline{in^2_{FET}})\,df\right)\Big/f_{3dB}\right)^{1/2}$$
$$= \left(\frac{4kT\cdot 2\pi f_{3dB}(C_{PD}+C_{gu}\cdot W)}{A} + \frac{4kT\cdot(2\pi)^2 f^2_{3dB}}{3}\times\left(\frac{P\cdot C^2_{PD}}{g_{mu}\cdot W}+\frac{(P-2Q+R)\cdot C^2_{gu}\cdot W}{g_{mu}} + \frac{2(P-Q)\cdot C_{gu}\cdot C_{PD}}{g_{mu}}\right)\right)^{1/2} \quad (8)$$

We selected the gate width of the input FET(Q_1) so as to get the minimum total input noise current ($\sqrt{\overline{in^2_t}}$), which is realized at a condition of

$$W = \left(\frac{2\pi f_{3dB}\cdot P\cdot A}{2\pi f_{3dB}\cdot(P-2Q+R)\cdot A + 3(g_{mu}/C_{gu})}\right)^{1/2}\cdot\left(\frac{C_{PD}}{C_{gu}}\right). \quad (9)$$

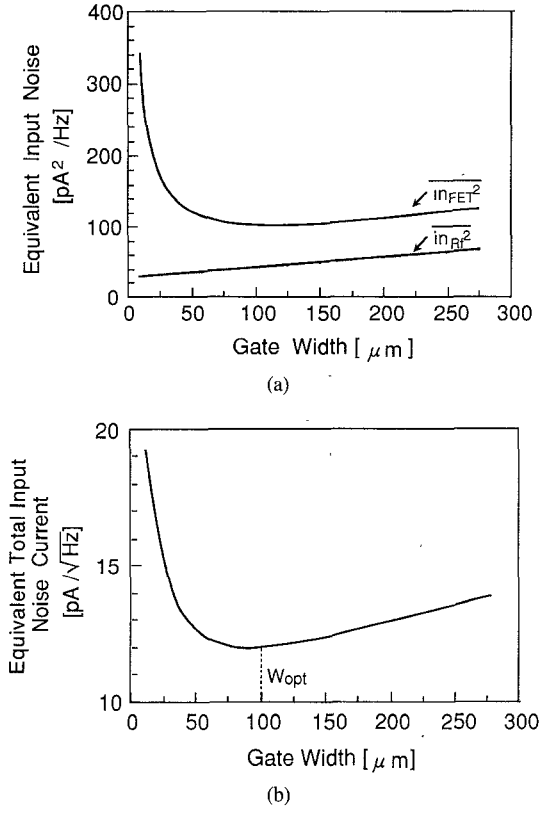


Fig. 2. (a) Two kinds of equivalent input noises ($\overline{in^2_{FET}}$ and $\overline{in^2_{Rf}}$) and (b) equivalent total input noise current ($\sqrt{\overline{in^2_t}}$) versus the gate width of FET(Q_1).

In Fig. 3, the 3 dB bandwidth (f_{3dB}) and equivalent input noise current ($\sqrt{\overline{in^2_{Rf}}}$) in the receiver are plotted against R_f obtained from SPICE with the GaAs MESFET model. The gate width of the input FET is 100 μm. In the design, f_{3dB} is chosen to be 7 GHz which is 70 percent of 10 Gb/s. In Fig. 3, f_{3dB} of 7 GHz is obtained for R_f of 400 Ω.

Shot noises due to the dark current in the p-i-n-photodiode ($\overline{in^2_d}$) and gate leakage current in the input FET ($\overline{in^2_g}$) are shown by the following equations [8], [9]:

$$\overline{in^2_d} = 2eI_d\Delta f \quad (10)$$

$$\overline{in^2_g} = 2eI_g\Delta f \quad (11)$$

where "e" is electron charge, I_d is dark current in the photodiode, and I_g is gate leakage current in the input FET(Q_1). Dark current in the InP p-i-n-photodiode is less than 100 nA and gate leakage noise in the input FET is an order of 0.1 to 1.0 μA for 100 μm gate width GaAs MESFET. Total shot noise is less than 0.5 pA^2/Hz and negligibly small compared with thermal noise of R_f.

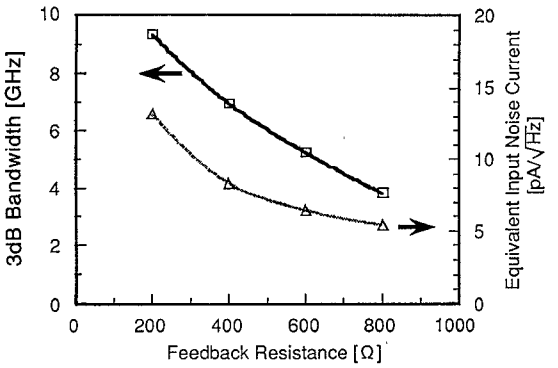


Fig. 3. 3-dB band-width and equivalent input noise current versus feedback resistance.

TABLE I
EACH COMPONENT SIZE OF THE IC

Element	Size
Q_1	100 μm
Q_2	200 μm
Q_3	200 μm
Q_4	400 μm
Q_5	200 μm
Q_6	200 μm
$D_1 \sim D_5$	100 μm
R_1	500 Ω
R_f	400 Ω
R_{out}	40 Ω

At the low frequency, $1/f$ noise ($\overline{in_{1/f}^2}$) is shown by the following equation,

$$\overline{in_{1/f}^2} = 4kTT \frac{(\omega \cdot C_t)^2}{g_m} \cdot \frac{f_c}{f} \Delta f \tag{12}$$

where f is frequency ($= \omega/2\pi$) and f_c is the $1/f$ noise corner frequency of the FET [8]. Because f_c is approximately 50 MHz for GaAs MESFET [8], $1/f$ noise can be neglected compared with the thermal noise of the input FET.

Each component of the IC shown in Fig. 1 is optimized using SPICE simulation except the input FET(Q_1). Table I shows the size of FET and diode and resistance in the IC after optimization. In the IC, we use resistive load because it has smaller noise contribution at the IC input than active load [9]. The load resistance (R_1) is 500 Ω. For the transconductance (g_m) of input FET(Q_1) which is an order of 10 mS, thermal noise of load resistor (R_1) is neglected by setting $R_1 >> 1/gm$ [10].

In the output buffer, because dc bias is over +2.5 V at the output port and V_{SS} is −5 V, dc voltage over 7 V is supplied between the output port and V_{SS}. Considering a breakdown voltage of each FET to be around 7 V, the output buffer is constructed by adding level-shift FET(Q_5) between the output port and drain of the FET(Q_6). Output impedance of the source follower FET(Q_4) of 400 μm gate width is approximately 10 Ω. To prevent reflection at the output port, the output impedance is matched to 50 Ω by connecting a resistor R_{out} of 40 Ω to the output terminal.

Fig. 4 shows the microphotograph of the IC. To realize a low noise and broadband preamplifier IC, we adopted the Self-Aligned Gate MESFET (SAGFET). The SAGFET has been developed for high speed GaAs LSI's, such as SRAM's [11] and gate arrays [12]. Because of excellent process controllability, the SAGFET leads to uniform preamplifier performance. The SAGFET has a Buried P-layer Lightly Doped Drain structure (BPLDD) fabricated by a 0.5 μm self-aligned WSi_x gate process [11]. Because a WSi gate has high sheet resistance compared with a conventional Au or Al gate, the effect of gate resistance on high frequency operation cannot be neglected and brings about degraded bandwidth and noise performance. Taking gate resistance into account the transimpedance and 3 dB bandwidth of the receiver are expressed as follows:

$$Z_{trans} = \frac{-R_f}{\left(\frac{j\omega C_g}{A}\right) \cdot \left(j\omega C_{PD} \cdot \left(R_g + \frac{1}{j\omega C_g}\right) \cdot R_f + R_f + \left(R_g + \frac{1}{j\omega C_g}\right)\right) + 1} \tag{13}$$

and

$$f_{3dB} \simeq \frac{A}{2\pi \left((C_{PD} + C_g) \cdot R_f + C_g \cdot R_g\right)} \tag{14}$$

respectively. Thermal noise in the gate resistance is expressed as

$$\overline{V_{R_g}^2} = 4kTR_g \Delta f \tag{15}$$

where R_g is gate resistance.

The effect of gate resistance can be neglected for the case that gate resistance is much smaller than the feedback resistance. Parallel connection of short gate fingers is effective to reduce the gate resistance of the FET. The distributed gate resistance (R_g) is expressed approximately [13] as follows:

$$R_g = R_\square \cdot \frac{W_u}{L_g \times N} \cdot \frac{1}{3} \tag{16}$$

where $R_\square$ is the sheet resistance of WSi gate metal (about 4 $\Omega/\square$), Lg is the gate length (0.5 μm), Wu is unit finger width, and N is the number of the fingers. Fig. 5 shows the measured and calculated R_g's versus gate width of the SAGFET for $N = 2$, 4, and 8. For $N = 4$, low R_g of 17.6 Ω has been obtained for gate width of 100 μm, which agrees well with an estimated value from (16).

As concerns the other device parameters, transconductance (g_m) and drain conductance (g_d) are 300 mS/mm and 6 mS/mm with standard deviations of 30 mS/mm and 0.7 mS/mm over a 3 inch wafer, respectively. The threshold voltage (V_{th}) of the FET is −0.5 V and its standard deviation (σV_{th}) is 30 mV.

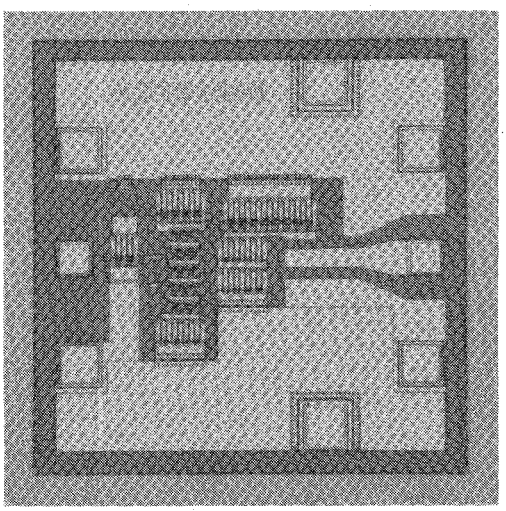


Fig. 4. Microphotograph of the preamplifier IC. (The chip size is 0.8 mm × 0.8 mm)

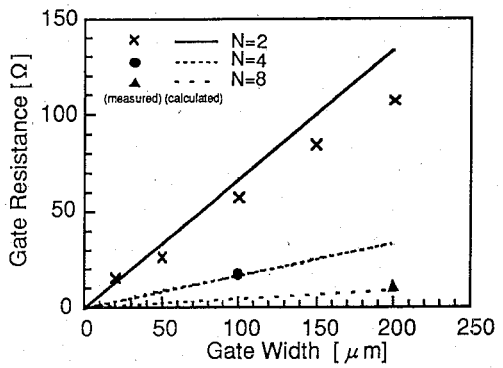


Fig. 5. Gate resistance (R_g) versus gate width of the SAGFET.

To simplify on-wafer RF measurements, a coplanar structure is employed for both input and output lines and two metal-insulator-metal capacitors are integrated as bypass capacitors for stabilizing the power supplies of +5 V and −5 V. The chip size is 0.8 mm × 0.8 mm.

Characteristics

Fig. 6 shows the *S*-parameters of the IC. The high gain |S21| of 9 dB and the broad bandwidth over 10 GHz have been obtained. Good matching has also been achieved. |S22| is less than −10 dB for the whole frequency range.

Fig. 7 shows the transimpedance characteristics of the IC calculated by using *S*-parameters. The high Z_{trans} of 44 dBΩ and the excellent broad bandwidth ($f_{3\,\text{dB}}$) of 12 GHz have also been obtained. The measured results show good agreement with those of the simulation. Fig. 8 shows the distribution of Z_{trans} and $f_{3\,\text{dB}}$ for a 3 inch wafer. Each standard deviation, σZ_{trans} and $\sigma f_{3\,\text{dB}}$, is as small as 0.2 dBΩ and 0.2 GHz, respectively. The uniform preamplifier performance comes from our excellent process controllability.

Fig. 9 shows the frequency response of a receiver that consists of the IC and an InP p-i-n photodiode. The diameter of the photodiode is 30 μm^{ϕ}, dark current is 30 nA

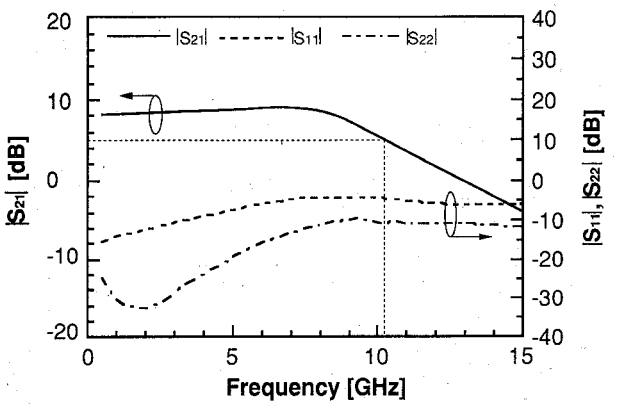


Fig. 6. *S*-parameters of the IC.

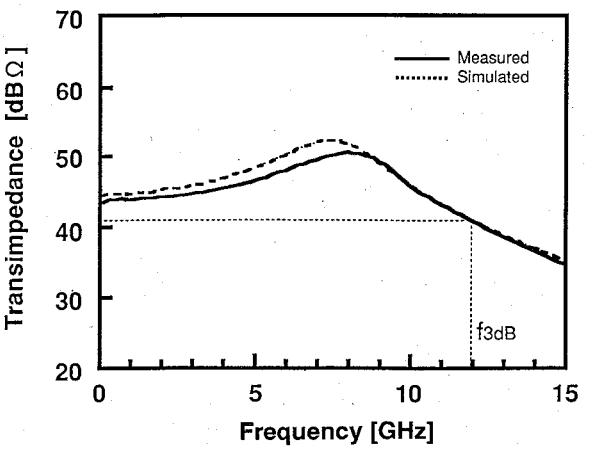


Fig. 7. Transimpedance characteristics of the IC.

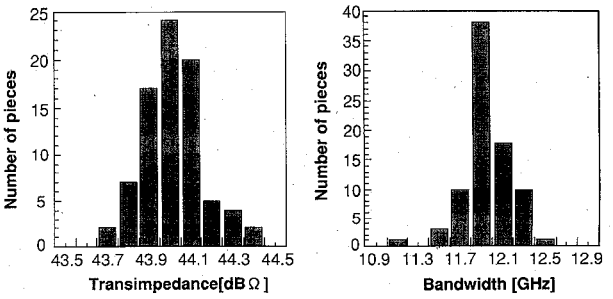


Fig. 8. Distribution of transimpedance and 3 dB bandwidth.

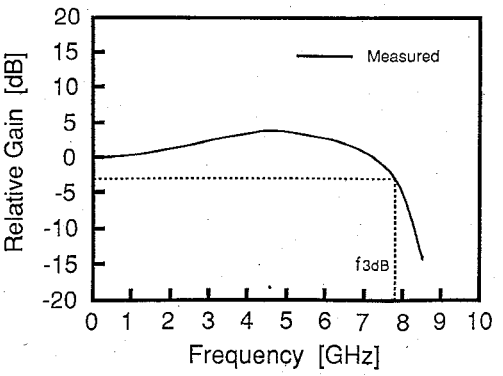


Fig. 9. Frequency response of the receiver.

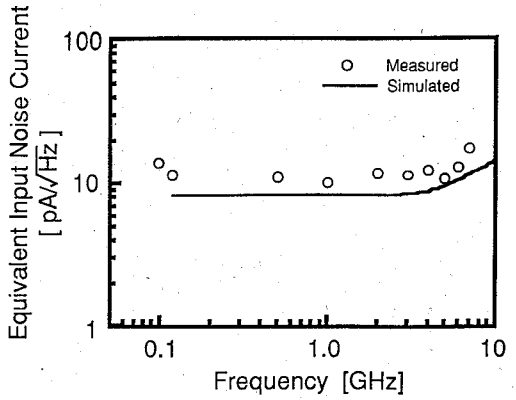


Fig. 10. Equivalent input noise current of the receiver.

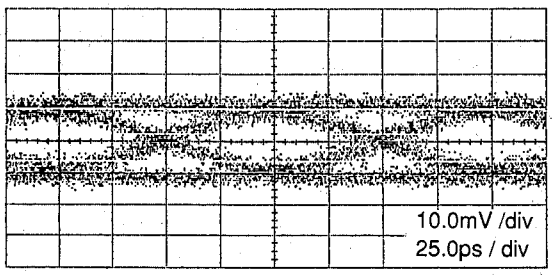


Fig. 11. Pulse response at 10 Gb/s NRZ signals of the receiver.

to 60 nA, the overall capacitance is 0.27 pF, and the 3 dB bandwidth is 15 GHz. To reduce the effect of parasitic capacitance and inductance added between the IC and the photodiode, bare chips are assembled on a ceramic carrier. A 3 dB bandwidth for the receiver of 7.8 GHz has been obtained, which satisfies our design target.

Fig. 10 shows noise performance. The equivalent input noise current $\sqrt{\overline{i_n^2}}$ of approximately 10 pA/$\sqrt{\text{Hz}}$ has been obtained over the entire frequency range from dc to 7.0 GHz. This indicates superior low noise performance of the IC.

Fig. 11 shows the pulse response at 10 Gb/s NRZ. Output voltage swing of 20 mVp-p corresponds to optical input power of −7.4 dBm. A good open eye pattern has been observed. These results suggest that the preamplifier IC developed in this work is suitable for a 10 Gb/s optical communication system.

Conclusion

An ultra broadband preamplifier IC using BPLDD SAGFETs having extremely short gate fingers has been designed and fabricated for a 10 Gb/s optical communication system. The IC shows high transimpedance of 44 dBΩ and broad bandwidth of 12 GHz. As a result of optimizing the gate width of the input FET and the feedback resistance, broad bandwidth of 7.8 GHz and an average low equivalent noise current of 12.6 pA/$\sqrt{\text{Hz}}$ have been obtained for a receiver with this preamplifier IC and a photodiode. The preamplifier IC developed in this work is suitable for a 10 Gb/s optical communication.

References

[1] N. Takachio, K. Iwashita, S. Hata, K. Katsura, K. Onodera, and H. Kikuchi, "A 10 Gb/s optical heterodyne detection experiment using a 23 GHz bandwidth balanced receiver," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1990, pp. 149–151.

[2] Y. Yamane, M. Ohhata, H. Kikuchi, K. Asai, and Y. Imai, "A 0.2 μm GaAs MESFET technology for 10 Gb/s digital and analog IC's," *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1991, pp. 513–516.

[3] N. Nagano, T. Suzaki, A. Okamato, and K. Honjo, "Monolithic ultra-broadband transimpedance amplifiers using AlGaAs/GaAs HBTs," *IEEE MTT-S Microwave Symp. Dig.*, June 1991, pp. 255–258.

[4] R. A. Minasian, "Optimum design of a 4-Gbit/s GaAs MESFET optical preamplifier," *IEEE J. Lightwave Technol.*, vol. LT-5, no. 3, pp. 373–379, Mar. 1987.

[5] K. Ogawa, "Noise Caused by GaAs MESFETs in Optical Receivers," *Bell Syst. Tech. J.*, pp. 923–928, July–Aug. 1981.

[6] W. Baechtold, "Noise Behavior of Schottky Barrier gate field-effect transistors at microwave frequencies," *IEEE Trans. Electron Devices*, vol. ED-18, no, 2, pp. 97–104, Feb. 1971.

[7] W. Baechtold, "Noise behavior of GaAs field-effect transistors with short gate lengths," *IEEE Trans. Electron Devices*, vol. ED-19, no. 5, pp. 674–680, May 1972.

[8] T. V. Muoi, "Receiver design for high-speed optical-fiber systems," *IEEE J. Lightwave Technol.*, vol. LT-2, no. 3, pp. 243–267, June 1984.

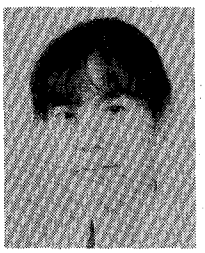
[9] Y. Archambault, D. Pavlidis, and J. P. Guet, "GaAs monolithic integrated optical preamplifier," *IEEE J. Lightwave Technol.*, vol. LT-5, no. 3, pp. 355–366, Mar. 1987.

[10] N. Scheinberg, R. J. Bayruns, and T. M. Laverick, "Monolithic GaAs transimpedance amplifiers for fiber-optic receivers," *IEEE J. Solid-State Circuits*, vol. 26, no. 12, pp. 1834–1839, Dec. 1991.

[11] M. Noda, K. Hosogi, K. Maemura, T. Kato, Y. Nakajima, K. Nishitani, and M. Outsubo, "High speed and highly uniform submicron gate BPLDDFET for GaAs LSIs," *Gallium Arsenide and Related Compounds*, pp. 653–658, 1989.

[12] N. Higashisaka, M. Shimada, T. Nishimura, N. Sasaki, M. Noda, H. Matsuoka, and S. Kayano, "A quasi-complementary-logic GaAs gate array employing air-bridge metallization technology," *IEEE CICC 1991*, 14.6.1–14.6.4.

[13] P. Wolf, "Microwave properties of Shottky-barrier field-effect transistor," IBM *J. Res. Develop.*, pp. 138–139, Mar. 1970.



Miyo Miyashita was born in Hyogo Pref., Japan, on October 11, 1964. She received the B.S. degree in physics from Kwansei-Gakuin University, Hyogo, Japan, in 1987.

She joined the Mitsubishi Electric Corporation, Itami, Japan, in 1987. Since then, she has been engaged in the research and development of high-speed GaAs ICs. Her present research interests include high-speed and high-frequency ICs for optical fiber transmission systems. She is currently a Technical Staff Member in the Microwave Device Development Department, Optoelectronic and Microwave Devices Laboratory, Itami, Japan.

Ms. Miyashita is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Kosei Maemura was born in Kumamoto Pref., Japan, on November 16, 1960. He received the B.S. degree in physics from Kumamoto University, Kumamoto, Japan, in 1983.

He joined the Mitsubishi Electric Corporation, Itami, Japan, in 1983. Since then, he has been engaged in the research and development of high-speed GaAs MSIs and LSIs. His present research interests include high-power amplifier ICs and modulator ICs for digital mobile communication systems, in addition to high-speed, high-frequency ICs for optical fiber transmission systems. He is currently a Technical Staff Member in the Microwave Device Development Department, Optoelectronic and Microwave Devices Laboratory, Itami, Japan.

Mr. Maemura is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Kazuya Yamamoto was born in Osaka Pref., Japan, on October 22, 1965. He received the B.S. and M.S. degrees in electrical engineering from the University of Osaka Prefecture, Osaka, Japan, in 1988 and 1990, respectively.

He joined the Mitsubishi Electric Corporation, Itami, Japan, in 1990. Since then, he has been engaged in the research and development of high-speed GaAs MSIs. His main interests include modulator ICs for digital mobile communication systems and high-speed, high-frequency ICs for optical fiber transmission systems. He is currently a Technical Staff Member in the Microwave Device Development Department, Optoelectronic and Microwave Devices Laboratory, Itami, Japan.

Mr. Yamamoto is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Teruyuki Shimura was born in Tokyo, Japan, on March 13, 1960. He received the B.S. degree in applied physics from the University of Tokyo, Tokyo, Japan, in 1983.

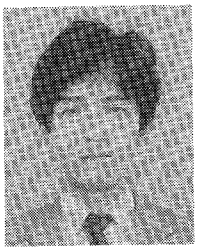
He joined the Mitsubishi Electric Corporation, Itami, Japan, in 1983. Since then, he has been engaged in the research and development of high-speed GaAs MSIs and LSIs. Since 1989, he has been engaged in the development of product engineering of AlGaAs/GaAs HBT ICs. He is currently a Technical Staff Member in the Microwave Device Development Department, Optoelectronic and Microwave Devices Laboratory, Itami, Japan.

Mr. Shimura is a member of the Japan Society of Applied Physics.

Masamichi Nogami was born in Yokohama, Japan on January 28, 1966. He is graduated from Toin Technical College, Kanagawa, Japan, in 1986.

In 1986, he joined the Mitsubishi Electric Corporation, Kamakura, Japan, where he has been engaged in the research and development of optical fiber transmission systems.

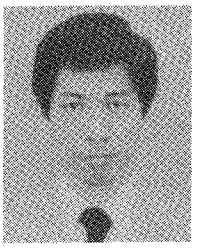
Mr. Nogami is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Kuniaki Motoshima was born in Nagasaki Pref., Japan on March 25, 1958. He received B.E. and M.E. degrees in electrical engineering from Tokyo University, Tokyo, Japan, in 1980 and 1982, respectively.

In 1982, he joined Mitsubishi Electric Corporation, Kamakura, Japan, where he has been engaged in the research and development of optical fiber transmission systems and equipments. He is currently the senior research engineer in Communication Systems Laboratory, Kamakura, Japan. He is now visiting to Center of Telecommunication Research, Columbia University. His main interests include optical amplifiers and there applications.

Mr. Motoshima is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Tadayoshi Kitayama was born in Kagawa, Japan on November 16, 1949. He received the B.E. and M.E. degrees in electrical engineering from Osaka University, Osaka, Japan, 1972 and 1974, respectively.

Since jointing Mitsubishi Electric Corporation, Japan, in 1974, he has been engaged in the research and development of optical fiber transmission systems and equipment. He research interests include optical amplification systems, Coherent Systems and Subcarrier Multiplexed Systems. He is currently the Manager of the Lightwave Transmission Group, in Communication Systems Laboratory, Kamakura, Japan.

Mr. Kitayama is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Yasuo Mitsui was born in Kobe, Japan, on April 29, 1949. He received the B.S. degree in applied physics and Ph.D. degree in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1972 and 1986, respectively.

He joined the Mitsubishi Electric Corporation, Tokyo, Japan in 1972. Since then, he has been engaged in the development of microwave semiconductor devices including Si TRAPATT diodes, a GaAs low-noise MESFET oscillator, GaAs high-power MESFETs, and GaAs ICs. His present research interests center on GaAs logic circuits and monolithic microwave ICs. He is currently the Manager of the Microwave Device Development Department, Optoelectronic and Microwave Devices Laboratory, Itami, Japan. Dr. Mitsui is a member of the Institute of Electronics, Information and Communication Engineers of Japan.